

**UNITED STATES DISTRICT COURT  
EASTERN DISTRICT OF TEXAS  
MARSHALL DIVISION**

|                                   |   |                              |
|-----------------------------------|---|------------------------------|
| NETLIST, INC.                     | ) |                              |
| Plaintiff,                        | ) |                              |
| v.                                | ) |                              |
|                                   | ) |                              |
| MICRON TECHNOLOGY, INC., MICRON   | ) | Civil Case No. 22-cv-203-JRG |
| SEMICONDUCTOR PRODUCTS, INC., and | ) |                              |
| MICRON TECHNOLOGY TEXAS LLC,      | ) | JURY TRIAL DEMANDED          |
| Defendants.                       | ) |                              |
|                                   | ) |                              |
|                                   | ) |                              |
|                                   | ) |                              |

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**JOINT 4-3 CLAIM CONSTRUCTION AND PREHEARING STATEMENT**

Pursuant to Local P.R. 4-3 and the Court’s Docket Control Order (Dkt. 40), Plaintiff Netlist, Inc. (“Netlist”) and Defendants Micron Technology Inc. (“Micron Technology”), Micron Semiconductor Products, Inc. (“Micron Semiconductor”), and Micron Technology Texas, LLC (“Micron Texas”) (collectively, “Micron”) submit this Joint Claim Construction and Prehearing Statement with regard to the following patents:

U.S. Pat. No 8,787,060 (the “’060 patent”);

U.S. Pat. No 9,318,160 (the “’160 patent”);

U.S. Pat. No 10,860,506 (the “’506 patent”);

U.S. Pat. No 10,949,339 (the “’339 patent”);

U.S. Pat. No 11,016,918 (the “’918 patent”); and

U.S. Pat. No 11,232,054 (the “’054 patent”).

**I. P.R. 4-3(a)(1): Agreed Constructions****A. '060, '160 patents**

| <b>Claim(s)</b>                                   | <b>Term</b>                                   | <b>Agreed Construction</b>                        |
|---|---|---|
| All asserted claims                               | "A memory package"                            | The preamble is limiting                          |
| All asserted claims                               | "array die"                                   | "array die that is different from a DRAM circuit" |
| '060 Patent, Claims 6, 11–14, 16–19, 20–21, 23–28 | "chip select signal" / "chip select conduits" | Plain and ordinary meaning                        |

**B. '506 patent**

| <b>Claim(s)</b> | <b>Term</b>   | <b>Agreed Construction</b> |
|-----------------|---|----------------------------|
| 1               | "A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising" | The preamble is limiting   |

**C. '339 patent**

| <b>Claim(s)</b> | <b>Term</b>   | <b>Agreed Construction</b>   |
|-----------------|---|--|
| 1-3, 11, 14     | “N-bit wide write data”   | “write data that is N bits in width”   |
| 1               | “A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising” | The preamble is limiting   |
| 11, 19          | “A N-bit-wide memory module mountable in a memory socket of a computer system and configured to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, the memory module comprising”   | The preamble is limiting   |
| 27              | “A memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and data signal lines, the data signal lines including a plurality of sets of data signal lines, each set of data signal lines is n bit wide, the memory module comprising”                                   | The preamble is limiting   |
| 1, 11, 34, 35   | “in accordance with a latency parameter”  | “a time period wherein the start of the time period depends on at least a latency parameter” |

**D. '918 and '054 patent**

N/A.

**II. P.R. 4-3(a)(2): Disputed Terms**

Exhibits A and B attached hereto contain the parties' proposed constructions for each disputed term, phrase, or clause together with the intrinsic and extrinsic evidence that the parties contend support their proposed constructions.

**III. P.R. 4-3(a)(3): Anticipated Length of Time for the Claim Construction Hearing**

The parties agree and expect that 3 hours will provide sufficient time to conduct the claim construction hearing.

**IV. P.R. 4-3(a)(4): Anticipated Witnesses at the Claim Construction Hearing**

The parties may present testimony from the parties' experts opining on claim construction issues in the form of written declarations and/or deposition testimony, to aid the Court in making its findings.

**V. P.R. 4-3(a)(5): Other Issues to be Addressed at the Claim Construction Hearing**

Currently, the parties do not believe that there are any other issues that might be appropriately addressed at a prehearing conference prior to the claim construction hearing.

Dated: May 2, 2023

Respectfully submitted,

/s/ Jason Sheasby

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**CERTIFICATE OF SERVICE**

I hereby certify that, May 2, 2023, a copy of the foregoing was served to all counsel of record.

/s/ Michael Tezyan  
Michael Tezyan